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SEMICONDUCTOR MODULE AND METHOD FOR FORMING THE SAME

Background of the Invention

1. Field of the Invention

[0001] The present invention generally relates to a semiconductor module and method for forming the same. Specifically, the present invention provides a semiconductor module having an interposer structure with metallurgical through connections for electrically connecting a semiconductor chip to a substrate.

2. Related Art

[0002] In the production of semiconductor modules, a semiconductor chip is often connected to a carrier such as a substrate. Typically, the connection is made using controlled collapse chip connection (C4) technology whereby solder bumps are used to join the two components together. Unfortunately, several problems emerge with the existing technology. First, the semiconductor chip usually has a different coefficient of thermal expansion (CTE) than the substrate. Given the close physical proximity of the semiconductor chip to the substrate, the solder bumps often deteriorate as the module heats up and cools off. This is especially the case with larger die sizes.

[0003] In addition, ceramic substrates (if used) are generally non-planar, which can become a gating factor as the substrate X-Y dimensions increase. With shrinking pitch, there is a need to shrink C4 bump dimensions to avoid nearest neighbor shorting. However, a small C4 bump height results in a larger percentage of variation across the

grid of bumps. Further, when the interconnections at the chip to substrate level migrate to a lead-free system, there will be no solder temperature hierarchy between first and second level interconnections, thus, creating an increased strain on the C4 structure due to higher temperatures of subsequent assembly operations. Still yet, current methods of depositing and joining C4 interconnections are expensive and involve the use of specific under bump metallization (UBM), which might have to be customized. Also, the UBM may need additional layers such as diffusion barriers and chip encapsulants so that it may endure a melting or partially melting C4 structure that reacts with the UBM during subsequent assembly operations.

[0004] In view of the foregoing, there exists a need for an improved semiconductor module and method for forming the same. Specifically, a need exists for a semiconductor chip to be electrically connected to a substrate or the like so that the above concerns are alleviated.

Summary of the Invention

[0005] In general, the present invention provides a semiconductor module and method for forming the same. Specifically, under the present invention, a semiconductor chip is electrically connected to a substrate (e.g., organic, ceramic, etc.) by an interposer structure. The interposer structure comprises an elastomeric, compliant material that includes metallurgical through connections having a predetermined shape. In a typical embodiment, the metallurgical through connections electrically connect an under bump metallization of the semiconductor chip to a top surface metallization of the substrate. By

utilizing the interposer structure in accordance with the present invention, the problems associated with previous semiconductor module designs are alleviated.

[0006] A first aspect of the present invention provides a semiconductor module, comprising a semiconductor chip; a substrate; and an interposer structure electrically connecting the semiconductor chip to the substrate, wherein the interposer structure includes metallurgical through connections having a predetermined shape.

[0007] A second aspect of the present invention provides a semiconductor module, comprising a semiconductor chip having an under bump metallization; a substrate having a top surface metallization; and an interposer structure electrically connecting the under bump metallization to the top surface metallization, wherein the interposer structure comprises an elastomeric, compliant material that includes metallurgical through connections having a predetermined shape.

[0008] A third aspect of the present invention provides a method for forming a semiconductor module, comprising: embedding metallurgical through connections within an elastomeric, compliant material to form an interposer structure; and positioning the interposer structure between a semiconductor chip and a substrate to electrically connect the semiconductor chip to the substrate.

[0009] Therefore, the present invention provides a semiconductor module and method for forming the same.

Brief Description of the Drawings

[0010] These and other features of this invention will be more readily understood from the following detailed description of the various aspects of the invention taken in conjunction with the accompanying drawings in which:

[0011] Fig. 1 depicts a semiconductor module having an interposer structure, according to the present invention.

[0012] Fig. 2 depicts the semiconductor module of Fig. 1 further including a heat spreader and a heat sink.

[0013] Fig. 3 depicts the semiconductor module of Fig. 2 further including underfill.

[0014] Fig. 4 depicts the semiconductor module of Fig. 3 under a Land Grid Array load.

[0015] Fig. 5 depicts the semiconductor module of Fig. 1 in a TCA application.

[0016] The drawings are merely schematic representations, not intended to portray specific parameters of the invention. The drawings are intended to depict only typical embodiments of the invention, and therefore should not be considered as limiting the scope of the invention. In the drawings, like numbering represents like elements.

Detailed Description of the Invention

[0017] As indicated above, the present invention provides a semiconductor module and method for forming the same. Specifically, under the present invention, a semiconductor chip is electrically connected to a substrate (e.g., organic, ceramic, etc.) by an interposer structure. The interposer structure comprises an elastomeric, compliant material that includes metallurgical through connections having a predetermined shape. In a typical

embodiment, the metallurgical through connections electrically connect an under bump metallization of the semiconductor chip to a top surface metallization of the substrate. By utilizing the interposer structure in accordance with the present invention, the problems associated with previous semiconductor module designs are alleviated.

[0018] Referring now to Fig. 1, an illustrative semiconductor module 10 formed in accordance with the present invention is shown. As depicted, semiconductor module 10 includes semiconductor chip 12 and carrier/substrate 14 with interposer structure 16 positioned therebetween. It should be appreciated in advance that semiconductor module 10 could be a single chip module or a multi-chip module. In the case of a multi-chip module, interposer structure 16 could be positioned between each semiconductor chip and substrate 14. Moreover, it should be understood that substrate 14 could be any type of substrate now known or later developed. For example, substrate 14 could be ceramic or organic. In any event, interposer structure 16 is positioned between semiconductor chip 12 and substrate 14 under the present invention to preserve the interface therebetween. As indicated above, differences in the CTE between semiconductor chip 12 (e.g., 3 ppm/^{0}C, CTE) and substrate 14 (15-18 ppm/^{0}C, CTE for an organic substrate) cause various issues as semiconductor module 10 is subjected to temperature change. Positioning interposer structure 16 between semiconductor chip 12 and substrate 14 increases the distance between the two components and alleviates the problems associated with the difference in CTEs.

[0019] In any event, interposer structure 16 generally comprises a elastomeric, compliant material 20 having metallurgical through connections 18 "embedded" or "positioned"

therein. Metallurgical through connections 18 electrically connect under bump metallization (UBM) or bottom layer metallurgy (BLM) 22 of semiconductor chip 12 to top surface metallurgy (TSM) 24 of substrate 14. In a typical embodiment, interposer structure 16 can comprise Cupil-T, which is commercially available from Nitto Denko, Inc. of Osaka, Japan. Moreover, metallurgical through connections 18 can be formed to have a predetermined shape depending on the load applied to semiconductor module 10 to best optimize the contact. For example, metallurgical through connections 18 could be spherical, ellipsoid, s-shaped, c-shaped, or elongate (i.e., column-like). various factors can be considered when determining the shape of metallurgical through connections 18. Such factors include, among other things: (1) camber (i.e., non-flatness of substrate 14 and semiconductor chip 12) in that more camber might mean taller through connections with an overall greater degree of compressibility; (2) distortion (i.e., positional accuracy of the I/O pads on substrate 14) in that the worse the distortion, the bigger the contact area on metallurgical through connections 18 that would have to be provided so that some degree of contact is always present between metallurgical through connections 18 and the I/O pads; and (3) process considerations such as how the through connections are made. In addition, metallurgical through connections 18 could be formed from one or more materials. To this extent, metallurgical through connections 18 could have a core formed from Copper, Copper-Beryllium, or the like that is coated with gold. Still yet, UBM 22 and/or TSM 24 could be gold, solder or the like.

[0020] To provide a more stable structure, interposer structure 16 could be rigidly attached (e.g., hard soldered) to either UBM 22 or TSM 24, or both. For example, if

semiconductor module 10 is placed under a Land Grid Array (LGA) load, metallurgical through connections 18 could be hard soldered to TSM 24, while the contact between metallurgical through connections 18 and UBM 22 is maintained solely by the LGA load. This would enable free expansion of the semiconductor chip side of interposer structure 16 under the influence of temperature. Since interposer structure 16 would not cause any strains due to TCE mismatch, the reliability of semiconductor module 10 would increase considerably. Further, this method would allow for self-aligned solder joining of metallurgical through connections 18 to the I/O pads on substrate 14, thus eliminating the concern of inadequate surface contact area when the I/O pad distortion is on the high end of the specification.

[0021] Referring now to Fig. 2, semiconductor module 10 of Fig. 1 further including a heat spreader 26 and heat sink 30 is shown. As depicted, heat spreader 26 is attached to semiconductor chip 12 using thermally conductive adhesive 28. To prevent the increased weight cause by heat spreader 26 and heat sink 30 from damaging semiconductor chip 12, substrate 14 and/or interposer structure 16, support posts 32A-B can be provided adjacent to interposer structure 16. Specifically, support posts 32A-B extend from substrate 14 to heat spreader 26, and support heat spreader 26 over semiconductor chip 12. It should be appreciated that the quantity of support posts 32A-B shown in Fig. 2 is intended to be illustrative only, and should not be limiting.

[0022] Regardless, to further seal interposer member 16 between semiconductor chip 12 and substrate 14, underfill could be provided. Specifically, referring to Fig. 3, semiconductor module 10 of Fig. 2 is shown as further including underfill 34. Under the

present invention, underfill 34 can be provided throughout the interconnection, or at predetermined locations. Further, underfill 34 can be a heat-curable material, selected from a broad range of chemical compositions including both rigid and flexibilized thermosetting epoxies, thermoplastics, urethanes, polysulfones, polyimides, polyetheramides/imides, and hybrids of same. Alternatively, underfill 34 can be a more compliant, thermoplastic material such as a silicone based product.

[0023] In any event, when underfill 34 is used, metallurgical through connections 18 could be rigidly attached to both UBM 22 and TSM 24 to provide a desired level of thermo-mechanical fatigue. To this extent, underfill 34 may be applied between interposer structure 16 and semiconductor chip 12, between interposer structure 16 and substrate 14, or between semiconductor chip 12 and substrate 14 (including interposer structure 16). In a typical embodiment, it is desirable to rigidly affix interposer structure 16 to substrate 14 whenever metallurgical through connections 18 are soldered to the substrate 14. In this case, a typical, high-modulus of elasticity underfill is indicated, e.g, materials having modulus ranging from 1 - 10 Giga Pascals. Similarly, yet another embodiment uses underfill 34 between semiconductor chip 12 and interposer structure 16 if metallurgical through connections 18 are permanently attached to the semiconductor chip 12.

[0024] In yet another embodiment of the invention, a more compliant, flexible, underfill material (having elastic modulus in the tens or hundreds of Mega Pascals, for example) is provided between the semiconductor chip 12 and substrate, including metallurgical through connections 18. This feature would allow lateral displacement of the electrical

contacts in response to thermally-induced stresses while preserving environmental protection of the IC devices(s) and joints.

[0025] Referring now to Fig. 4, semiconductor module 10 of Fig. 3 under an LGA load is shown. Under an LGA load, forces are exerted on semiconductor module 10 in the direction of the arrows shown. As indicated above in conjunction with Fig. 1, metallurgical through connections 18 could be rigidly attached to TSM 24 under such a load. Referring to Fig. 5, semiconductor module 10 under a Temporary Chip Attachment (TCA) application is depicted. Under a TCA application, a porous surface is provided for vacuum pickup and/or placement of semiconductor chip 10. Accordingly, as can be seen, interposer structure 16 can be used within semiconductor modules 10 in a variety of scenarios and applications. In addition, although not shown herein, interposer structure 16 could be used as a fan-out layer so that a very fine pitch in UBM 22 may be connected to a more coarse pitch in substrate 14.

[0026] The foregoing description of the preferred embodiments of this invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and obviously, many modifications and variations are possible. Such modifications and variations that may be apparent to a person skilled in the art are intended to be included within the scope of this invention as defined by the accompanying claims. For example, in another embodiment, interposer structure 16 could be integrated at the wafer level (e.g., 8 or 12 inch wafers) and electrically tested before chip singulation (e.g., dicing) is performed.